

# **Triangular Sorters: A VLSI Systolic Architecture For Sorting (GIT-ICS) By Pin-Yee Chen**

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## **Patent us5541914 - packet-switched self-routing**

Packet-switched self-routing multistage interconnection network having system and its advantages over a VLSI Why systolic architectures

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## **Patent us4639857 - digital data processor**

Digital data processor incorporating an orthogonally connected logic of  $l \times m$  processing cells adjacent to a triangular sub Systolic Arrays (for VLSI),

## **Parallel processing, part 2 - university of**

Sorting Networks Proof of Batcher s Even-Odd Merge Batcher s Even-Odd Merge Sorting Example Batcher s Even-Odd 8-Sorter Systolic Data Structures 8.3

## **Patent us4799152 - pipeline feedback array sorter**

The feedback array sorter further includes a merge tree array having  $q$  leave nodes connected to the output of said first buffer memory,

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FOREWORD The VHSIC Program is currently in its seventh year, with only a few more challenging years to go. DoD and the Services have made tremendous strides in all of

## **Parallel implementation of the double bracket**

Parallel Implementation of the Double Bracket Matrix Flow for Eigenvalue-Eigenvector Computation upper triangular of the systolic array in VLSI.

## **Presentation "winter 2014parallel processing,**

Winter 2014Parallel Processing, Circuit-Level ParallelismSlide 1 Part II Circuit-Level Parallelism Part II Circuit-Level Parallelism 7.

## **International journal of advanced research in**

International Journal of Advanced Research in Proximity Coupled Equilateral Triangular Microstrip Design and Implementation of VLSI 8 Bit Systolic

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- . . ,mn 0 01 05\_1 1 10 100 10th 11 11\_d0003 12 13 14 141a 143b 15 16 17 17igp 18 19 1900 1901 1902 1903 1904 1905 1906 1907 1908 1909 1910 1911 1912 1913 1914 1915

## **Modulo 3 residue checker - association for**

Research Triangle Institute, "A bit-serial VLSI architectural An algorithm-based fault tolerance is achieved by testing the invariants of a systolic sorter

## **Sceas**

Real-time adaptive signal processing using a dynamic reconfigurable systolic architecture in analog VLSI. through triangular noise sorters for multiplier

## **The enigma that is poppinpooper - adult swim**

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## **Slide 1**

anaLOG: A functional Simulator for VLSI Neural Systems. Trace Theory and Systolic Computations. Images, Numerical Analysis of Singularities and Shock Filters.

## **Ieee xplore - conference table of contents**

2014 IEEE International Symposium on; Circuits and In the analog VLSI implementation as well as the QRD-based triangular systolic array but

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## **2010 ieee asia pacific conference on circuits and**

VLSI implementation of a fast intra prediction algorithm for H.264/AVC encoding Systolic-array 3D wave-digital beam filters Panning sorter:

## **On the design of a high-performance, expandable,**

expandable and high-performance sorter based on of the sorter and its size. A systolic-type architecture zero time" VLSI sorter, IBM

## **Patent us4493048 - systolic array apparatuses for**

Systolic array apparatuses for matrix computations /a and the said array computes the solution of a triangular linear Systolic VLSI array for

## **Handbook of sensors and actuators - scribd**

HANDBOOK OF SENSORS AND ACTUATORS Series Editor: VLSI and Intelligent Transducers, shown in Figure 2, and 3-D systolic arrays, for example,

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Insertion Sorter Unit It sorts a Triangular systolic array with reduced latency for QR the 20th International Conference on VLSI Design jointly with the

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Circuits and Systems, IEEE Transactions on ( 1963 - 1973 VLSI architectures. The sorter, and the design of a

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Bibliographic content of IEEE Transactions on Computers, Volume 39. A VLSI DEsign for Computing Systolic Architectures for the Computation of the Discrete

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A critique of network speed in VLSI models of square and triangular decompositions are described for different designs for VLSI sorters.

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Proving (facts about) Ruby logic for describing and reasoning about systolic arrays. Taking triangular arrays as of a systolic sorter is formally

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e.g., triangular array, Bit-serial VLSI implementation of delayed LMS adaptive FIR filters: A systolic implementation of the Chan/Foster RRQR algorithm:

**Presentation "spring 2006parallel processing,**

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EditionReleasedRevised FirstSpring 2005Spring 2006 This presentation is intended to

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